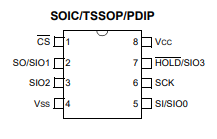
23LC1024 Serial SRAM Driver Notes

Datasheet available at https://docs.rs-online.com/5f59/0900766b8114ca33.pdf

3 Modes of SPI are available via commands (default is extended (1-bit))

## Pinout



This is the pinout for the chip – in SPI Extended mode, only Pin 5 (serial in) and Pin 2 (serial out) are used for data transfer.

In Extended and SDI mode, the HOLD\_n input (pin 7) must be driven HIGH to allow for data transfer

We need bidirectional buffers on pins 2, 3, 5 and 7.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Pin | Pin Name | Description | FPGA Direction | XDC Connection |
| 1 | CS\_n | Chip Select (n) | out | JA(7) |
| 2 | SO/SIO1 | Serial Out/Serial InOut1 | In/inout | JA(6) |
| 3 | SIO2 | Serial InOut2 | inout | JA(5) |
| 4 | Vss | GND | N/A | GND |
| 5 | SI/SIO0 | Serial In/Serial InOut0 | Out/inout | JA(1) |
| 6 | SCK | SPI Clock | out | JA(2) |
| 7 | HOLD\_n/SIO3 | Hold Transaction (n)/Serial Inout3 | Out/inout | JA(3) |
| 8 | Vcc | 2V5 – 5V5 | N/A | 3V3 |

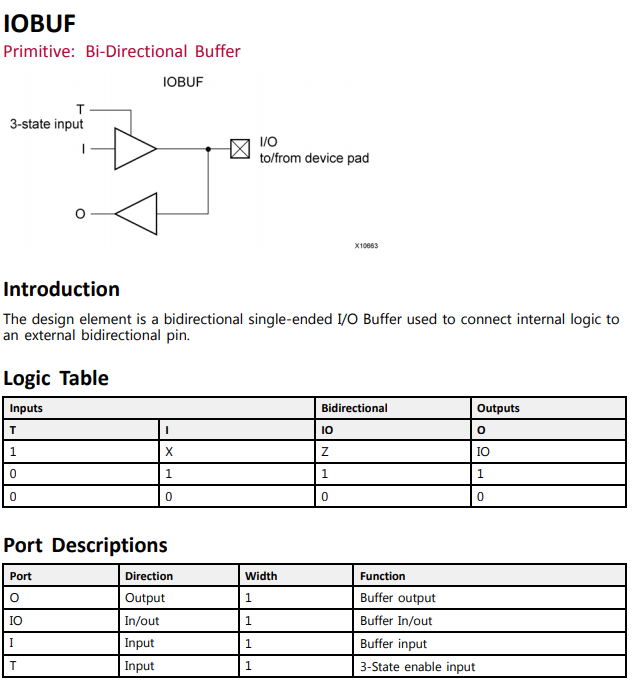
|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| PMOD Pin | FPGA Pin | FPGA XDC Connection | 23LC1024 Pin | Fixed 23LC1024 Pin |
| JA1 | J1 | JA(0) |  | CS# |
| JA2 | L2 | JA(1) | Pin 5 SI/SIO0 | SI/SIO0 |
| JA3 | J2 | JA(2) | Pin 6 SCK | SO/SIO1 |
| JA4 | G2 | JA(3) | Pin 7 HOLD\_n/SIO3 | SCK |
| JA5 (GND) | GND |  |  |  |
| JA6 (PWR) | PWR |  | Pin 8 Vcc |  |
| JA7 | H1 | JA(4) |  | SIO2 |
| JA8 | K2 | JA(5) | Pin 3 SIO2 | HOLD#/SIO3 |
| JA9 | H2 | JA(6) | Pin 2 SO/SIO1 |  |
| JA10 | G3 | JA(7) | Pin 1 CS\_n |  |
| JA11 (GND) | GND |  | Pin 4 Vss |  |
| JA12 (PWR) | PWR |  |  |  |

Pmod pin mapping: **NOTE use FIXED PIN mappings above**

A screen shot of a computer

Description automatically generated

# Artix-7 Primitives



Controller Operation